REMARKS

In response to the Office Action mailed March 2, 2009, Applicants respectfully request reconsideration. Claims 1-8 and 12 were previously pending in this application. By this paper, no claims have been added or amended. As a result, claims 1-8 and 12 are pending for examination with claims 1, 5, 7, and 8 being independent. No new matter has been added.

Claim Rejections - 35 USC § 101

The Office Action rejected claims 1-4 and 12 under 35 U.S.C. 101 as allegedly directed to non-statutory subject matter. In particular, the Office Action states that claims 1-4 and 12 "recite an 'assembler' comprising a series of elements that, viewed in light of the specification, can be reasonably interpreted as software, per se. The claims do not define any structural and functional interrelationships between the software elements and a computer that would permit the described functionality to be realized when the software is employed as a computer component."

Applicants respectfully note that claim 1 recites an assembler **for a target microprocessor** (emphasis added). Thus, contrary to the assertions made in the Office Action, claim 1 does not merely recite "functional descriptive material" or "nonfunctional descriptive material." Further, claim 1 recites the assembler comprising a descriptor file containing information **descriptive of the instruction set of said target microprocessor** ... (emphasis added). Thus, a target microprocessor which is a hardware element is recited in claim 1. In addition, claim 1 recites that the assembler automatically tracks changes in the instruction set ... . Therefore, operation of the assembler as recited in claim 1 depends on the instruction set of the target microprocessor. Thus, clam 1 does not recite descriptive material *per se*.

Rejections under 35 U.S.C. §112

The Office Action rejected claims 1-8 and 12 under 35 U.S.C. 112, first paragraph, as "failing to comply with the enhancement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention." Applicants respectfully disagree.

A. Brief Summary of the Specification

As an aid to the Examiner, Applicants provide a brief summary of the specification of the present application. This summary is not intended as a substitute for the Examiner's reading of the application in its entirety. Also, the summary is not intended to characterize the claims or terms used in the claims.

Briefly, the present specification is directed to generating an assembler for a target microprocessor. The specification addresses a problem related to preparation of programs for microprocessors which are still in a process of development (page 1, lines 24-26). During the development of such microprocessors, their instruction set may be altered which may take the form of altering the size and location of instruction operands or the writing of new instructions (page 1, lines 26-29). Thus, an assembler that is typically a program that translates instructions comprising mnemonics and operands into binary representations must ensure that the binary representation of operands are located in the correct bit fields (page 1, lines 31-33 and page 2, lines 3-5). This is typically achieved by hard coding of control information into the assembler program (page 2, lines 5-6).

The specification describes avoiding the need for hard coding of control information for each new instruction set architecture by providing a descriptor file (page 2, lines 21-31). The descriptor file contains information descriptive of the instruction set of the target microprocessor (page 2, lines 30-31). Examples of the descriptor file are shown in Figs. 4 and 6 and discussed on page 11, particularly, on lines 2-13.

In operation of the assembler described in the present specification, a fetch unit 23 addresses the descriptor file 24 and provides output information representative of constraints due to the instruction set architecture (page 9, lines 8-12). The output information is applied to a control device 26 which operates on the translated information such that is conforms which the requirements of the instruction set (page 9, lines 12-15).

The source code is translated in a manner which automatically takes into account data from the descriptor file which represents the current instruction set architecture (page 8, lines 30-32). If the instruction set architecture changes, the descriptor file 24 can be altered and thus the assembler can (without hard coding) take into account the changes in the instruction set architecture by accessing, via fetch unit 24, the new descriptor file. Thus, the assembler

automatically takes into account the instruction set architecture. When the instruction set architecture changes, the descriptor file is changed (manually or automatically) accordingly and the assembler operates to track the changes using fetch unit 23 and control device 25.

Figs. 4 and 6 show how respective tables are related to instructions shown in Figs. 3 and 5, respectively, and that a descriptor file can be created from a particular instruction set architecture.

B. The claims are supported by Applicants' specification

On page 5, the Office Action states that the "'automatic' embodiment of applicants' disclosure includes the use of utility program 31 to access instruction set architecture data 30 to provide the descriptor file 24." Applicants respectfully note that, as described in the brief summary of the specification provided solely as an aid to the Examiner, the automatic tracking of changes in the instruction set architecture is related to using a fetch unit 23 that addresses the description file 23 such that the output of the translation device 21 of the assembler is used to constrain the output to conform with the requirements of the instruction set.

On page 6, the Office Action asserts that "the steps necessary to carry out the manipulation and inspection of the instruction set are not described with any particularity such that this procedure can be easily automated through software."

Accordingly, withdrawal of the rejection of claims 1-8 and 12 under 35 U.S.C. §112 is respectfully requested. Applicants respectfully note that one of skill in the art would be able to take information on instruction set architecture automatically and create a description file. Applicants' specification provides, with reference to Figs. 3 and 6, some examples of this procedure on pages 11 and 13.

Further, on page 6, the Office Action asserts " [t]he only detailed description of the descriptor file appears to be the diagrammatic illustrations in Figs. 4 and 6. However, these figures illustrate tables and do not suggest a particular file structure." Applicants respectfully submit that one of skill in the art would realize how to create a file structure using a table. As described in the brief summary of the specification, Figs. 4 and 6 show how respective tables are related to instructions shown in Figs. 3 and 5, respectively, and that a descriptor file can be created from a particular instruction set architecture. Description of the figures is provided on pages 11 and 12 of Applicants' specification.

In view of the above, "automatically" tracking changes in instruction set architecture of a target microprocessor is supported in Applicants' specification.

Accordingly, withdrawal of the rejection of claims 1-8 and 12 under 35 U.S.C. 112, first paragraph, is respectively requested.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, the Director is hereby authorized to charge any deficiency or credit any overpayment in the fees filed, asserted to be filed or which should have been filed herewith to our Deposit Account No. 23/2825, under Docket No. S1022.80572US00.

Dated: July 2, 2009

Respectfully submitted,

By: _____

James H. Morris, Reg. 34,681
WOLF, GREENFIELD & SACKS, P.C.
Federal Reserve Plaza
600 Atlantic Avenue
Boston, Massachusetts 02210-2206
617.646.8000